SOLID STATE IMAGING DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

This application is based upon and claims the benefit of priority from Japanese Patent Application No. 2015-177513; filed on September 9, 2015; the entire contents of which are incorporated herein by reference.

FIELD

Embodiments described herein relate generally to a solid state imaging device.

BACKGROUND

It is known that a solid state imaging device includes a pixel cell which is configured by a plurality of pixels. The plurality of pixels of the pixel cell share configuration elements of the pixel with each other. In the solid state imaging device, if there is a certain malfunction in a configuration element which is shared by a plurality of pixels, abnormality can occur in a signal output of each pixel in the pixel cell.

The solid state imaging device may perform flaw correction for a pixel which is registered as a correction target in advance. The solid state imaging device corrects flaw which is a defect of a signal from the pixel through signal processing. The solid state imaging device stores positional information of a target pixel which becomes a target of correction in a memory. It is preferable that the solid state imaging device reduces information retained for the target pixel and thereby a size of a circuit for correction processing can be reduced.

An example of related art includes Japanese Patent No. 5541718.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a solid state imaging device according to a first embodiment.

FIG. 2 is a block diagram of a camera system including the solid state imaging device illustrated in FIG. 1.

FIG. 3 is a schematic diagram illustrating pixel cells which are arranged in a pixel region illustrated in FIG. 1.

FIG. 4 is a block diagram of a flaw correction circuit illustrated in FIG. 1.

FIG. 5 is a schematic diagram illustrating target pixels for flaw correction and pixels around the target pixels in the flaw correction circuit illustrated in FIG. 4.

FIG. 6 is a schematic diagram illustrating a modification example of the pixel cells which are arranged in the pixel region illustrated in FIG. 1.

FIG. 7 is a block diagram of a flaw correction circuit which is included in the solid state imaging device according to a second embodiment.

FIG. 8 is a schematic diagram illustrating target pixels for flaw correction and pixels around the target pixels in the flaw correction circuit illustrated in FIG. 7, and pixels around the target pixels.

FIG. 9 is a block diagram of the flaw correction circuit included in the solid state imaging device according to the second embodiment.

DETAILED DESCRIPTION

[0005]An exemplary embodiment provides a solid state imaging device in which a size of a configuration for correction processing can be reduced.

[0006]In general, according to one embodiment, a solid state imaging device includes a pixel region and a correction circuit. Pixel cells are arranged in a row direction and a column direction, in the pixel region. The pixel cell includes a plurality of pixels. The correction circuit performs correction processing on a signal from the pixel. The correction circuit includes a memory. The memory retains positional information of a target pixel. The target pixel is a target of correction processing. The memory retains positional information of a representative pixel for the plurality of target pixels that are included in the pixel cell. The representative pixel is one of the plurality of target pixels.

[0008]A solid state imaging device according to the present embodiment will be hereinafter described with reference to the accompanying drawings. The invention is not limited to the embodiments.

First Embodiment

[0009]FIG. 1 is a block diagram of a solid state imaging device according to a first embodiment. FIG. 2 is a block diagram of a camera system including the solid state imaging device illustrated in FIG. 1. The camera system 1 is an electronic apparatus including a camera module 2, and a camera-equipped mobile terminal. The camera system 1 may be an electronic apparatus such as a digital camera.

[0010]The camera system 1 includes the camera module 2 and a post-stage processing unit 3. The camera module 2 includes an imaging optical system 4 and a solid state imaging device 5. The post-stage processing unit 3 includes an image signal process (ISP) 6, a recording unit 7, and a display unit 8.

[0011]The imaging optical system 4 receives light from a subject. The imaging optical system 4 includes an imaging lens (not illustrated) focuses a subject image. The solid state imaging device 5 images a subject image. The solid state imaging device 5 is a complementary metal oxide semiconductor (CMOS) image sensor. The solid state imaging device 5 may be a charge coupled device (CCD).

[0012]The ISP 6 performs signal processing on an image signal from the solid state imaging device 5. The ISP 6 performs various signal processing such as, demosaic processing, white balance adjustment, color matrix processing, or gamma correction. The recording unit 7 records an image which is obtained by signal processing performed by the ISP 6, in a recording medium or the like. The recording unit 7 outputs an image signal to the display unit 8 according to an operation of a user.

[0013]The display unit 8 displays an image according to an image signal from the ISP 6, or an image signal which is read from the recording unit 7. The display unit 8 is, for example, a liquid crystal display. The camera system 1 performs a feed-back control of the camera module 2, based on the data which is obtained by signal processing of the ISP 6.

[0014]The solid state imaging device 5 includes a pixel region 11, a control circuit 12, a row scanning circuit 13, a column scanning circuit 14, a column processing circuit 15, and an imaging processing circuit 16. The pixel region 11 includes pixel cells which are arranged in a row direction and a column direction. The pixel cell includes a plurality of pixels. The pixel includes a photo diode which is an electro-optical conversion element. The electro-optical conversion element generates signal charges in accordance with an incident light amount. The pixel accumulates the signal charges which are generated according to the incident light amount. The pixel region 11 outputs the pixel signal in accordance with the incident light amount to the pixel.

[0015]The control circuit 12, the row scanning circuit 13, the column scanning circuit 14, the column processing circuit 15, and the imaging processing circuit 16 configure a peripheral circuit that is integrated in a chip in which the pixel region 11 is formed. Various data and blocks for driving the solid state imaging device 5 are supplied to the control circuit 12 through the imaging processing circuit 16 from the ISP 6 in the outside of the chip.

[0016]The control circuit 12 generates various pulse signals for controlling drive of a peripheral circuit portion, in response to a clock signal. The control circuit 12 supplies pulse signals indicating driving timing to each of the row scanning circuit 13, the column scanning circuit 14, the column processing circuit 15, and the imaging processing circuit 16.

[0017]The row scanning circuit 13 includes a shift register, an address decoder, or the like. The row scanning circuit 13 that is a pixel drive circuit supplies the pixels of the pixel region 11 with a drive signal. The control circuit 12 supplies the row scanning circuit 13 with a pulse signal in accordance with a vertical synchronization signal. The row scanning circuit 13 sequentially selects pixel rows from which pixel signals are read, according to the pulse signals from the control circuit 12. The row scanning circuit 13 performs read scanning by sequentially supplying read signals to each pixel in the selected pixel row. The read signals are drive signals for reading pixel signals generated according to an incident light amount, from the pixels.

[0018]The row scanning circuit 13 performs read scanning in accordance with supply of reset signals to each pixel, prior to supply of the read signals to each pixel. The reset signals are drive signals for discharging charges remaining in an electro-optical conversion element. Each pixel accumulate signal charges which are generated according to an incident light amount, during a period from when the reset signals are supplied until the read signals are supplied.

[0019]The drive signals are transmitted from the row scanning circuit 13 to each pixel through pixel drive lines 17. The pixel drive lines 17 are provided in each pixel row of the pixel region 11. The pixel rows are configured by pixels which are arranged in a row direction (horizontal direction).

[0020]The pixel signals are transmitted from each pixel to the column processing circuit 15 through vertical signal lines 18. The vertical signal lines 18 are provided in each column of the pixel cell.

[0021]The column processing circuit 15 performs processing on the pixel signals which are transmitted through the vertical signal lines 18, in unit circuits (not illustrated). The unit circuits are provided in each pixel cell. The column processing circuit 15 performs correlated double sampling (CDS) processing for reducing fixed pattern noise, with respect to the pixel signals. The column processing circuit 15 performs an AD conversion of converting a pixel signal that is an analog signal into a digital signal. The column processing circuit 15 may perform processing other than the CDS and AD conversion. The column processing circuit 15 retains the pixel signals which are obtained through the CDS and AD conversion, in each unit circuit.

[0022]The column scanning circuit 14 includes a shift register, an address decoder, and the like. The control circuit 12 supplies the column scanning circuit 14 with a pulse signal in accordance with a horizontal synchronization signal. The column scanning circuit 14 sequentially selects the pixel columns from which the pixel signals are output, according to the pulse signal from the control circuit 12. The column processing circuit 15 sequentially outputs retained in each unit circuit, according to select scanning performed by the column scanning circuit 14.

[0023]The imaging processing circuit 16 performs processing on the pixel signals from the column processing circuit 15. The imaging processing circuit 16 includes a flaw correction circuit 19. The flaw correction circuit 19 is a correction circuit which performs flaw correction processing on the pixel signals. The flaw correction circuit 19 corrects flaw in which positional information is registered in advance, and performs so-called map flaw correction.

[0024]The imaging processing circuit 16 may be configured in various types to perform signal processing, in addition to the flaw correction circuit 19. The imaging processing circuit 16 performs the flaw correction based on a result of flaw determination which is performed by using a signal value of the pixel, and may include a configuration for so-called direct flaw correction. The imaging processing circuit 16 may include a configuration for black level correction, gamma correction, noise reduction, lens shading correction, white balance adjustment, distortion correction, resolution reconstruction, or the like.

[0025]The solid state imaging device 5 outputs a RAW image signal that is a signal through signal processing performed by the imaging processing circuit 16 to the outside of the chip. The camera system 1 may perform the signal processing which is performed by the solid state imaging device 5 according to the present embodiment, in a circuit other than a peripheral circuit portion of a chip which is the same as the pixel region 11. The signal processing may be performed by, for example, the ISP 6 of the post-stage processing unit 3, instead of the peripheral circuit portion. The camera system 1 may perform the signal processing which is performed by the peripheral circuit portion, in both the peripheral circuit and the ISP 6. The peripheral circuit and the ISP 6 may perform signal processing other than the signal processing described in the present embodiment.

[0026]FIG. 3 is a schematic diagram illustrating pixel cells which are arranged in a pixel region illustrated in FIG. 1. The X direction and the Y direction are respectively a row direction and a column direction in the pixel region 11. A pixel cell 20 is configured by four pixels which are arranged in the Y direction.

[0027]In FIG. 3, “R”, “G”, and “B” respectively represent a red (R) pixel, a green (G) pixel, and a blue (B) pixel. The R pixel is a pixel which detects red light. The G pixel is a pixel which detects green light. The B pixel is a pixel which detects blue light. The R pixel, the G pixel, and the B pixel respectively include a color filter (not illustrated). The R pixel includes a color filter through which red light selectively passes. The G pixel includes a color filter through which green light selectively passes. The B pixel includes a color filter through which blue light selectively passes.

[0028]In the pixel region 11, the respective pixels of R, G, and B configure Bayer arrangement. The pixel region 11 includes the pixel cell 20 including the G pixel and the B pixel, and the pixel cell 20 including the R pixel and the G pixel.

[0029]Four pixels which configure the pixel cell 20 share a MOS transistor that is a configuration element of a pixel. The four pixels configure a pixel sharing structure of a so-called 4V1H. The four pixels share, for example, a transfer transistor that is a MOS transistor, a floating diffusion (FD), a reset transistor, an amplification transistor, and a row select transistor.

[0030]The pixel cell 20 includes four photo diodes (PD) that are electro-optical conversion elements for each pixel. The PD generates signal charges in accordance with incident light amount. The transfer transistor transmits the signal charges from the PD to the FD, in response to a read signal that is a drive signal from the row scanning circuit 13. The FD converts the signal charges which are transmitted by the transfer transistor, into potential.

[0031]The amplification transistor amplifies a potential change of the FD to set as a pixel signal. The reset transistor discharges charges of the FD in response to a reset signal that is a drive signal from the row scanning circuit 13, and initializes the potential of the FD to a constant level. The solid state imaging device 5 has a pixel sharing structure, and thus a pixel pitch can be reduced, compared to a case in which the MOS transistors are disposed in each pixel.

[0032]FIG. 4 is a block diagram of the flaw correction circuit illustrated in FIG. 1. The flaw correction circuit 19 includes an average value calculation circuit 21, an one time programmable memory (OTP) 22, a flaw determination circuit 23, and a selector 24. The average value calculation circuit 21, the flaw determination circuit 23 and the selector 24 are configured by appropriately combining various logic circuits and storage elements for retaining calculation results and various data. The storage element may be one of a register and a memory.

[0033]The flaw correction circuit 19 includes a horizontal delay line (not illustrated) which performs delay of a pixel unit with respect to a pixel signal which is input. The average value calculation circuit 21 receives signal values of the same color pixels in the same row as a target pixel that is a target for flaw correction. The same color pixels are set as pixels which detect the same color light as the target pixel. The average value calculation circuit 21 is a calculation circuit which calculates an average value Ax of the signal value which is input.

[0034]The OTP 22 is a memory which retains positional information of the target pixel. The flaw determination circuit 23 grasps timing when a signal value from the target pixel is input to the selector 24, based on a pulse signal from the control circuit 12 and positional information that the OTP 22 retains. The flaw determination circuit 23 supplies the selector 24 with a control signal in accordance with the timing when the signal value from the target pixel is input to the selector 24.

[0035]The selector 24 selects one of the pixel signal from the horizontal delay line and the average value Ax from the average value calculation circuit 21. The selector 24 selects the average value Ax from the average value calculation circuit 21 in response to the control signal from the flaw determination circuit 23, with respect to the target pixel. The selector 24 selects the pixel signal from the horizontal delay line with respect to pixels other than the target pixel. The flaw correction circuit 19 outputs the signal selected by the selector 24.

[0036]Adjustment processing for storing the positional information of the target pixel to the OTP 22 is performed in an inspection process at the time of manufacturing, for example, the solid state imaging device 5. In the adjustment processing, a test for detecting flaw from the pixel region 11 is performed. The OTP 22 stores the positional information which is set based on the test results.

[0037]Subsequently, a specific example of flaw correction performed by the flaw correction circuit 19 will be described. FIG. 5 is a schematic diagram illustrating target pixels for flaw correction in the flaw correction circuit illustrated in FIG. 4, and pixels around the target pixel.

[0038]As the pixel cell 20 has a defect in an element which is shared by four pixels, for example, the FD, abnormality can occur in a signal output from each pixel. The solid state imaging device 5 employs a pixel sharing structure, and thus the entire pixels of the pixel cell 20 can be flawed by a defect of one portion of the pixel cell 20. Since multiple flaws are created together, the flaws are easily noticed in an image, compared to flaws which are created in a dispersed manner for each pixel. Hatched pixel cell 20 in FIG. 5 illustrates a state in which both two G pixels and two B pixels are flawed.

[0039]The flaw correction circuit 19 performs flaw correction in which the entire pixels in the pixel cell 20 become target pixels, and flaw correction in which a flaw of one pixel unit becomes a target. It is assumed that the flaw of one pixel unit is created by defects other than the defect of the pixel sharing element.

[0040]Here, information of the target pixels which are stored in the OTP 22 will be described by classifying into a case in which the entire pixels in the pixel cell 20 are target pixels, and a case other than that. As an example of a case other than flaw correction in which the entire pixels in the pixel cell 20 are set as target pixels, flaw correction of two pixel flaws will be described. The two pixel flaws are assumed to mean that flaws of one pixel unit are created in two pixels with same color which are adjacent to each other.

[0041]The OTP 22 retains an address which is positional information of one flaw, and identification information representing a disposition aspect of the two pixel flaws, as information on the two pixel flaws. The flaw determination circuit 23 seeks an address of the other flaw, based on the address and the identification information of the one flaw. The flaw correction circuit 19 performs flaw correction in which the two pixels with same color are set as target pixels. Calculation of a correction value will be described later. The identification information is set as a unique numeric value which is set for each disposition aspect.

[0042]The OTP 22 retains an address which is positional information of one representative pixel in the pixel cell 20, and identification information indicating that the entire pixels in the pixel cell 20 are set as target pixels, as information of a case in which the entire pixels in the pixel cell 20 are set as target pixels.

[0043]In the pixel cell 20 illustrated in FIG. 5, “G0” that is one G pixel is designated as a representative pixel. “G0” is a pixel which is read earliest, among four pixels in the pixel cell 20. The OTP 22 retains an address of “G0” and identification information indicating that the entire pixels in the pixel cell 20 are set as target pixels, with respect to target pixels which are the four pixels in the pixel cell 20. The identification information is set as a unique numeric value other than the numeric value set for the aforementioned two pixels.

[0044]The flaw determination circuit 23 grasps that the entire pixels in the pixel cell 20 in which “G0” is set as a representative pixel are target pixels, based on the address of “G0” and the identification information. The flaw determination circuit 23 seeks addresses of three target pixels other than “G0” in the pixel cell 20. As a method of representing address by using XY coordinates in which a pixel is set as a unit, if position of “G0” is represented by (x,y), the flaw determination circuit 23 obtains (x,y+1), (x,y+2), and (x,y+3) with regard to the other three target pixels.

[0045]If the four target pixels in the pixel cell 20 are regarded as two sets, each having two pixels, the OTP 22 can retain two sets of a combination of positional information and identification information, with respect to one pixel cell 20. In the present embodiment, it is sufficient for the OTP 22 retain one set of a combination of the positional information and the identification information with respect to one pixel cell 20, and thus it is possible to reduce the amount of information which is retained in the OTP 22. The solid state imaging device 5 can reduce the capacity of the OTP 22, and manufacturing cost.

[0046]The average value calculation circuit 21 calculates an average value of signal values of “Gx1” and “Gx2”, with respect to “G0” which is one target pixel. “Gx1” and “Gx2” are G pixels which are arranged in the same row as “G0”, and are pixels which have the same color as “G0” and are adjacent to “G0” in which one R pixel with different color is interposed therebetween in the X direction. “Gx1” and Gx2” are positioned in (x-2,y) and (x+2,y).

[0047]The average value calculation circuit 21 calculates an average value of a signal value VGx1 of “Gx1” and a signal value VGx2 of “Gx2”, using the following expression (1).

Ax=(VGx1+VGx2)/2 ××××× (1)

[0048]The selector 24 receives a signal value VG0 of “G0” from the horizontal delay line, and receives the average value Ax that is a correction value for “G0” from the average value calculation circuit 21. The selector 24 selects the average value Ax in response to a control signal from the flaw determination circuit 23.

[0049]The average value calculation circuit 21 calculates average values for the three target pixels other than “G0”, in the same manner as “G0”. The average value calculation circuit 21 calculates an average value of the signal value of the G pixel disposed in the same row as “G1”, when “G1” that is the G pixel other than “G0” in the pixel cell 20 is the target pixel. The flaw correction circuit 19 does not need a configuration for delaying a pixel signal by a row unit, by using a signal value of a pixel with the same color which is disposed in the same row as the target pixel to calculate a correction value. The flaw correction circuit 19 can perform correction processing, using a relative simple circuit configuration.

[0050]The average value calculation circuit 21 also calculates an average value for the target pixel of one pixel unit, in the same manner as a case in which the entire pixels in the pixel cell 20 are set as target pixels. The flaw correction circuit 19 also performs flaw correction for the target pixel of one pixel unit, in the same manner as a case in which the entire pixels in the pixel cell 20 are set as target pixels.

[0051]The average value calculation circuit 21 may calculate the average value by using an expression other than expression (1) described above. In addition, the pixel region 11 is not limited to arrangement of the pixel cell 20 of 4V1H. The number of pixels included in one pixel cell may be appropriately changed.

[0052]FIG. 6 is a schematic diagram illustrating a modification example of the pixel cells which are arranged in the pixel region illustrated in FIG. 1. A pixel cell 25 according to the modification example includes eight pixels which form a matrix of two pixel in the Y direction and four pixel in the X direction. The eight pixels configure a so-called pixel sharing structure of 4V2H. The OTP 22 retains one set of a combination of positional information and identification information with respect to one pixel cell 25. The solid state imaging device 5 can reduce the amount of information which is retained in the OTP 22.

[0053]The pixel arrangement of the pixel region 11 may be pixel arrangement other than the Bayer arrangement. The present embodiment can also be employed to a configuration in which pixel cells are arranged with regard to pixel arrangement other than the Bayer arrangement, and thus the solid state imaging device 5 can reduce the amount of information which is retained in the OTP 22.

[0054]According to the first embodiment, the flaw correction circuit 19 retains the positional information on the representative pixel in the OTP 22, with respect to the target pixels that are a plurality of pixels which configure the pixel cell. The solid state imaging device 5 can reduce the amount of information, which is retained in the OTP 22, on the target pixels. As a result, the solid state imaging device 5 can obtain effect in which a size of a configuration for correction processing can be reduced.

Second Embodiment

[0055]FIG. 7 is a block diagram of a flaw correction circuit which is included in the solid state imaging device according to a second embodiment. The same symbols or reference numerals will be attached to the same units as those of the first embodiment, and repetitive description thereof will be appropriately omitted.

[0056]A the flaw correction circuit 30 includes a line memory 31, average value calculation circuits 32 and 33, subtracters 34 and 35, an average value determination circuit 36, a register 37, the OTP 22, the flaw determination circuit 23, and the selector 24. The average value calculation circuits 32 and 33 and the average value determination circuit 36 are configured by appropriately combining various logic circuits and a storage element for retaining calculation results and various data. The storage element may be one of a register and a memory.

[0057]Te line memory 31 retains pixel signals in a row unit. The line memory 31 temporarily retains the pixel signals, and thereby the pixel signals are delayed in each row of the pixel region 11. The line memory 31 retains signals of six pixel rows. The line memory 31 is, for example, an SRAM. The flaw correction circuit 30 includes a horizontal delay line (not illustrated) which delays the pixel signal from the line memory 31 in a pixel unit.

[0058]The average value calculation circuits 32 and 33 are calculation circuits which calculate average values of signal values which are input. The subtracters 34 and 35 are logic circuits which perform substration of the signal values which are input. The average value determination circuit 36 is an average value determination circuit which determines one of the average values which becomes a correction value, from the average values calculated by the average value calculation circuits 32 and 33. The register 37 is a storage element which retains a threshold that is used for determination of the average value determination circuit 36. The threshold may be stored in a storage element other than the register 37, for example, a memory.

[0059]The selector 24 selects one of the pixel signal from the horizontal delay line and a correction value from the average value determination circuit 36. The selector 24 selects the correction value from the average value determination circuit 36 in response to a control signal from the flaw determination circuit 23, for a target pixel. The selector 24 selects the pixel signal from the horizontal delay line, for pixels other than the target pixel. The flaw correction circuit 30 outputs a signal selected by the selector 24.

[0060]Subsequently, a specific example of flaw correction performed by the flaw correction circuit 30 will be described. FIG. 8 is a schematic diagram illustrating target pixels for flaw correction in the flaw correction circuit illustrated in FIG. 7, and pixels around the target pixels.

[0061]The average value calculation circuit 33 calculates an average value of signal values of “Gx1” and “Gx2”, with respect to “G0” which is one target pixel. “Gx1” and “Gx2” are positioned in (x-2,y) and (x+2,y). The average value calculation circuit 33 calculates a first average value Ax which is an average value of a signal value VGx1 of “Gx1” and a signal value VGx2 of “Gx2”, using the aforementioned expression (1), in the same manner as the average value calculation circuit 21 according to the first embodiment.

[0062]The average value calculation circuit 32 calculates an average value of signal values of “Gy1” and “Gy2”, with respect to “G0” which is one target pixel. “Gy1” and “Gy2” are G pixels which are arranged in the same column as that of “G0”. “Gy1” is a pixel which has the same color as “G0” and is adjacent to “G0” in which one B pixel with different color is interposed therebetween in the Y direction. “Gy2” is a pixel which has the same color as “G0” and is positioned across three pixels in the Y direction in the pixel cell 20 from “G0”. “Gy1” and “Gy2” are respectively positioned in (x,y-2) and (x,y+4).

[0063]The average value calculation circuit 32 calculates a second average value Ay which is an average value of a signal value VGy1 of “Gy1” and a signal value VGy2 of “Gy2”, using the following expression (2).

Ay=(VGy1+VGy2)/2 ××××× (2)

[0064]The subtracter 35 calculates a difference value Da which is obtained by subtracting a first average value Ax calculated by the average value calculation circuit 33 from a second average value Ay calculated by the average value calculation circuit 32 (Da=Ay-Ax). The difference value Da represents a difference between brightness in the Y direction and brightness in the X direction.

[0065]The subtracter 34 calculates a difference value Dy between the second average value Ay calculated by the average value calculation circuit 32 and a signal value VGy1 of “Gy1” (Dy=|Ay-VGy1|). The difference value Dy represents the amount of changes of brightness of a vertical direction (Y direction) of the pixel cell 20 including “G0”. The difference value Dy may be a difference value between the signal value VGy1 of “Gy1” and a signal value VGy2 of “Gy2”.

[0066]The register 37 retains a first threshold Ty and a second threshold Ta. Ty and Ta are registered in the register 37 when the solid state imaging device 5 is manufactured. Ty and Ta which are stored in the register 37 may also be changed according to a setting operation to the camera system 1, an imaging mode, or the like.

[0067]The average value determination circuit 36 compares the difference value Dy and the first threshold Ty. The difference value Dy represents the amount of changes of brightness in the Y direction around the pixel cell 20. The average value determination circuit 36 determines whether or not the brightness in the Y direction is the same as each other from the comparison results of Dy and Ty.

[0068]The average value determination circuit 36 compares the difference value Da and the second threshold Ta. The difference value Da represents a difference between the brightness in the X direction around “G0” and the brightness in the Y direction around the pixel cell 20. The average value determination circuit 36 determines whether or not the brightness in the Y direction is sufficiently great, compared to the brightness in the X direction from the comparison results of Da and Ta.

[0069]The average value determination circuit 36 determines that the brightness in the Y direction around the pixel cell 20 is the same as each other, if Dy is less than Ty (Dy<Ty). The average value determination circuit 36 determines that the brightness in the Y direction is sufficiently great compared to the brightness in the X direction, if Da is greater than Ta (Da>Ta).

[0070]As Dy<Ty and Da>Ta are satisfied, the average value determination circuit 36 determines that a line-shaped pattern having sufficient brightness with respect to periphery exists along the pixel cell 20 including “G0” in the Y direction. The average value determination circuit 36 determines that the second average value Ay is a correction value, if Dy<Ty and Da>Ta are satisfied. The average value determination circuit 36 employs the second average value Ay calculated from image information in the Y direction as a correction value for “G0”.

[0071]If Dy is greater than or equal to Ty (Dy³Ty) or Da is less than or equal to Ta (Da£Ta), the average value determination circuit 36 determines that the line-shaped pattern does not exist along the pixel cell 20 including “G0” in the Y direction. If one of Dy³Ty and Da£Ta is satisfied, the average value determination circuit 36 determines that the first average value Ax is the correction value. The average value determination circuit 36 employs the first average value Ax calculated from image information in the X direction as a correction value for “G0”.

[0072]the selector 24 receives a signal value VG0 of “G0” from the horizontal delay line, and receives the first average value Ax or the second average value Ay that are correction values for “G0” from the average value determination circuit 36. The selector 24 selects the first average value Ax or the second average value Ay from the average value determination circuit 36 in response to a control signal from the flaw determination circuit 23.

[0073]The flaw correction circuit 30 also performs calculation of the average value performed by the average value calculation circuits 32 and 33 and the determination performed by the average value determination circuit 36, for the three target pixels other than “G0”. The average value calculation circuit 32 uses the signal value of “G0” in which the flaw correction is performed, for calculation of the second average value, when “G1” that is the G pixel in the pixel cell 20 including “G0” is a target pixel. In addition to this, the average value calculation circuit 32 may use an average value of the signal values “Gy1” and “Gy2” which are sought when “G0” is the target pixel, as the second average value when “G1” is a target pixel.

[0074]If a bright line exists along the pixel cell 20 in the Y direction, a correction value is sought on the basis of the signal values of the pixels with the same colors in the X direction with respect to each target pixel in the pixel cell 20, and thereby the line in a portion of the pixel cell 20 can be removed. In addition, if the correction value is obtained by using the signal values of the pixels with the same color in a two-dimensional direction of the X direction and the Y direction in the same manner, it is possible to calculate the correction value to which brightness information from others except the line are greatly reflected compared to the brightness information on the line. In this case, it is possible to significantly reduce brightness of the line in a portion of the pixel cell 20.

[0075]If it is determined that there is a bright line along the pixel cell 20 in the Y direction in accordance with the determination of the average value determination circuit 36, the flaw correction circuit 30 employs the second average value calculated from the image information in the Y direction to a correction value. The flaw correction circuit 30 reduces erasing of the line in the portion of the pixel cell 20, and a significant decrease of the brightness of the line. The flaw correction circuit 30 can reduce image degradation due to correction processing for each target pixel of the pixel cell 20.

[0076]The average value calculation circuits 32 and 33 may calculate the average value by using expressions other than the expressions (1) and (2). The average value determination circuit 36 may determine the correction value, using a method other than the comparison of the difference value Dy and the first threshold Ty, and the comparison of the difference value Da and the threshold Ta.

[0077]The flaw correction circuit 30 may also perform the flaw correction for a target pixel of one pixel unit, using the same method as a case in which the entire pixels in the pixel cell 20 are set as target pixels.

[0078]According to the second embodiment, the flaw correction circuit 30 can reduce image degradation due to correction processing, by determining the correction value using the average value determination circuit 36. The solid state imaging device 5 can obtain an image with high quality. In addition, the solid state imaging device 5 reduce the amount of information, which is retained in the OTP 22, on the target pixels, in the same manner as in the first embodiment. As a result, the solid state imaging device 5 can obtain effects in which a size of the configuration for correction processing can be reduced and an image with high quality can be obtained.

Third Embodiment

[0079]FIG. 9 is a block diagram of the flaw correction circuit included in the solid state imaging device according to the second embodiment. The same symbols or reference numerals will be attached to the same units as those of the first embodiment, and repetitive description thereof will be appropriately omitted.

[0080]A flaw correction circuit 40 includes the average value calculation circuit 21, the OTP 22, the selector 24, a register 41, and a flaw determination circuit 42. The register 41 is a storage element which is used for retaining the thresholds Tvb and Tvw that are used for determination of the flaw determination circuit 42. The thresholds Tvb and Tvw may be retained in a storage element other than the register 41, for example, a memory.

[0081]The flaw determination circuit 42 compares a signal value of a target pixel from the horizontal delay line with the thresholds Tvb and Tvw. The flaw determination circuit 42 supplies the selector 24 with a control signal, based on the comparison results and positional information stored in the OTP 22. The flaw determination circuit 42 determines whether or not to exclude each pixel in the pixel cell 20 including a representative pixel from a target for correction processing, based on a signal value of the representative pixel. The flaw determination circuit 42 is configured by appropriately combining various logic circuits with a storage element for retaining calculation results and various data. The storage element may be one of a register and a memory.

[0082]Subsequently, a specific example of flaw correction performed by the flaw correction circuit 40 will be described. Here, a case in which each pixel of the pixel cell 20 in which “G0” illustrated in FIG. 5 is set as a representative pixel is registered as a correction target will be used as an example.

[0083]The flaw determination circuit 42 compares the signal value VG0 of “G0” with the thresholds Tvb and Tvw. The flaw determination circuit 42 compares the signal value VG0 with the threshold Tvb, thereby determining whether or not “G0” corresponds to black flaw, in analog gain conditions and electronic shutter time of the solid state imaging device 5 at the time of imaging. The black flaw represents a low signal level compared to the time when a pixel normally functions.

[0084]The flaw determination circuit 42 compares the signal value VG0 with the threshold Tvw, thereby determining whether or not “G0” corresponds to white flaw, in analog gain conditions and electronic shutter time of the solid state imaging device 5 at the time of imaging. The white flaw represents a high signal level compared to the time when a pixel normally functions.

[0085]If the signal value VG0 is greater than the threshold Tvb (VG0>Tvb), the flaw determination circuit 42 determines that “G0” does not correspond to the black flaw. If the signal value VG0 is less than the threshold Tvw (VG0<Tvw), the flaw determination circuit 42 determines that “G0” does not correspond to the white flaw. If Tvb<VG0<Tvw is satisfied, the flaw determination circuit 42 determines that “G0” does not correspond to both the black flaw and the white flaw, in the analog gain conditions and electronic shutter time at the time of imaging. The flaw determination circuit 42 stops supply of the control signal to the selector 24 with respect to “G0”. The selector 24 selects the signal value VG0 with respect to “G0”.

[0086]As Tvb<VG0<Tvw is satisfied with regard to “G0” which is a representative pixel, the flaw determination circuit 42 regards that the other three pixels in the pixel cell 20 do not correspond to both the black flaw and the white flaw. The flaw determination circuit 42 also stops supply of the control signal to the selector 24, with respect to the three pixels. The selector 24 also selects signal values of each pixel, with respect to the three pixels.

[0087]If the signal value VG0 is less than or equal to the threshold Tvb (VG0£Tvb), the flaw determination circuit 42 determines that “G0” corresponds to the black flaw. If the signal value VG0 is greater than or equal to the threshold Tvw (VG0³Tvw), the flaw determination circuit 42 determines that “G0” corresponds to the white flaw. As VG0£Tvb or VG0³Tvw is satisfied, the flaw determination circuit 42 determines that “G0” corresponds to the black flaw or the white flaw, in the analog gain conditions and electronic shutter time at the time of imaging. The flaw determination circuit 42 supplies the control signal to the selector 24 with respect to “G0”. The selector 24 selects the average value Ax that is a correction value with respect to “G0”.

[0088]As VG0£Tvb or VG0³Tvw is satisfied with regard to “G0” which is a representative pixel, the flaw determination circuit 42 regards that the other three pixels in the pixel cell 20 correspond to the black flaw or the white flaw. The flaw determination circuit 42 also supplies the control signal to the selector 24, with respect to the three pixels. The selector 24 also selects the average value Ax that is a correction value with respect to the three pixels.

[0089]In this way, if it is determined that “G0” does not correspond to the flaw, the flaw determination circuit 42 excludes each pixel of the pixel cell 20 including “G0” from the target of flaw correction. If the flaw determination circuit 42 determines that “G0” corresponds to the flaw, the flaw correction circuit 40 performs the flaw correction in which each pixel of the pixel cell 20 including “G0” is set as target pixels.

[0090]Even though each pixel of the pixel cell 20 is registered as targets of flaw correction, if flaw is not noticed in the analog gain conditions and electronic shutter time at the time of imaging, the flaw correction circuit 40 treats signal values of each pixel as normal values. Since the signal values of the target pixels remain depending on situation at the time of imaging, the flaw correction circuit 40 can further reduce an influence on image quality due to no correction processing. In addition, the flaw correction circuit 40 can prevent resolution from decreasing due to averaging of signals performed by correction processing. As a result, the solid state imaging device 5 can obtain an image with high quality depending on situation at the time of imaging.

[0091]The thresholds Tvb and Tvw are registered in the register 41 when the solid state imaging device 5 is manufactured. The threshold Tvb is a fixed value which is set as an upper limit of brightness for the black flaw. The threshold Tvw is a fixed value which is set as a lower limit of brightness for the white flaw. The thresholds Tvb and Tvw are not respectively limited to the fixed values. The thresholds Tvb and Tvw may be functions which use one of analog gain and electronic shutter time at the time of imaging, as a variable. Te flaw determination circuit 42 compares the thresholds Tvb and Tvw which are obtained by assigning a parameter to the variable, with the signal value of the representative pixel.

[0092]The flaw correction circuit 40 may also perform the flaw correction using the same method as in a case in which the entire pixels in the pixel cell 20 are set as the target pixels, for the target pixel of one pixel unit. The flaw correction circuit 40 may combine the flaw determination circuit 42 and the register 41 according to the present embodiment with the configuration of the second embodiment.

[0093]According to the third embodiment, the flaw determination circuit 42 determines whether or not to exclude each pixel in the pixel cell 20 including the representative pixel from the target of correction processing, based on the signal value of the representative pixel. The flaw correction circuit 40 can suppress the correction processing for the flaw which is not noticed depending on situation at the time of imaging. The solid state imaging device 5 can obtain an image with high quality depending on the situation at the time of imaging. In addition, the solid state imaging device 5 can reduce the amount of information, which is retained in the OTP 22, on the target pixel, in the same manner as in the first embodiment. As a result, the solid state imaging device 5 can obtain effects in which a size of the configuration for correction processing can be reduced and an image with high quality can be obtained.

[0094]While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

WHAT IS CLAIMED IS:

1. A solid state imaging device comprising:

a pixel region in which pixel cells having a plurality of pixels are arranged in a row direction and a column direction; and

a correction circuit which performs correction processing on a signal from the pixel,

wherein the correction circuit includes a memory which retains positional information of a target pixel which is set as a target of correction processing, and

wherein the memory retains positional information of a representative pixel which is one of a plurality of target pixels, for the plurality of target pixels that are included in the pixel cell.

2. The device according to Claim 1, wherein the memory retains positional information of the representative pixel, and identification information which indicates that each pixel in a pixel cell including the representative pixel is a target pixel.

3. The device according to Claim 1 or 2,

wherein the correction circuit includes a calculation circuit which calculates a correction value for the target pixel, and

wherein the calculation circuit calculates an average value of signal values of the pixels which are disposed in the same row as that of the target pixel.

4. The device according to Claim 1 or 2,

wherein the calculation circuit calculates a first average value which is an average value of signal values of the pixels that are disposed in the same row as that of the target pixel, and a second average value which is an average value of signal values of the pixels that are disposed in the same column as that of the target pixel, and

wherein the correction circuit includes an average value determination circuit which determines an average value that is set as a correction value for the target pixel from the first average value and the second average value.

5. The device according to Claim 4, wherein the average value determination circuit determines that the second average value is the correction value, if the amount of changes of brightness around the pixel cell including the target pixel in a column direction is less than a first threshold, and a difference between brightness in the column direction and brightness around the target pixel in a row direction is greater than a second threshold.

6. The device according to any one of Claims 1 to 5, wherein the correction circuit includes a correction determination circuit which determines whether or not to exclude each pixel in the pixel cell including the representative pixel from a target for correction processing, based on a signal value of the representative pixel.

ABSTRACT

According to one embodiment, a solid state imaging device includes a pixel region and a flaw correction circuit that is a correction circuit. Pixel cells are arranged in a row direction and a column direction, in the pixel region. The pixel cell includes a plurality of pixels. The correction circuit performs correction processing on a signal from the pixel. The correction circuit includes an OTP that is a memory. The memory retains positional information of a target pixel. The target pixel is a target of correction processing. The memory retains positional information of a representative pixel for a plurality of target pixels that are included in the pixel cell. The representative pixel is one of the plurality of target pixels.

FIG. 1

5: SOLID STATE IMAGING DEVICE

13: ROW SCANNING CIRCUIT

11: PIXEL REGION

12: CONTROL CIRCUIT

15: COLUMN PROCESSING CIRCUIT

14: COLUMN SCANNING CIRCUIT

16: IMAGING PROCESSING CIRCUIT

19: FLAW CORRECTION CIRCUIT

FIG. 2

1: CAMERA SYSTEM

2: CAMERA MODULE

4: IMAGING OPTICAL SYSTEM

5: SOLID STATE IMAGING DEVICE

3: POST-STAGE PROCESSING UNIT

7: RECORDING UNIT

8: DISPLAY UNIT

FIG. 4

19: FLAW CORRECTION CIRCUIT

21: AVERAGE VALUE CALCULATION CIRCUIT

23: FLAW DETERMINATION CIRCUIT

FIG. 7

30: FLAW CORRECTION CIRCUIT

31: LINE MEMORY

32: AVERAGE VALUE CALCULATION CIRCUIT

33: AVERAGE VALUE CALCULATION CIRCUIT

36: AVERAGE VALUE DETERMINATION CIRCUIT

23: FLAW DETERMINATION CIRCUIT

FIG. 9

40: FLAW CORRECTION CIRCUIT

21: AVERAGE VALUE CALCULATION CIRCUIT

42: FLAW DETERMINATION CIRCUIT